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10/581,754	06/05/2006	Cheng Zheng	42P23020	8501

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,754	ZHENG ET AL.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2009*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to amended claims 1, 7, 12, and 25 have been considered but are moot in view of the new ground(s) of rejection. In view of Applicant's amendments, a new ground of rejection is being presented further in view of Garthwaite et al. (US 7,389,385).

Garthwaite et al. teaches compacting a heap memory to remove gaps between live memory objects (Col. 2, lines 35-41) wherein the process of compacting the heap, an object may be relocated to a destination location that causes the object to span two destination blocks after compaction (see Col. 18, lines 20-24; Claim 3; and Figure 6B showing a compacted heap and object 310C spanning block 320A and 320B, object 310F spanning block 320B and 320C, and object 310I spanning block 320D and 320E). In the system of Garthwaite et al. each object contains a single header (see object 450 of Figure 4B) even when stored spanning two blocks of the heap.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 6-8, 12-13, and 25-26 are rejected under 35 U.S.C. 103(a) as being obvious over Eilert (US 6,909,645) in view of Sinclair (US 2007/0088904) further in view of Garthwaite et al. (US 7,389,395).

Regarding Claim 1, Eilert discloses a memory device comprising: an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable phase change memory, Col. 1, line 65 – Col. 2, line 6); and control circuitry coupled with the array of memory locations (processors 52 as shown in Figure 4).

Eilert does not disclose a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Eilert to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Eilert in view of Sinclair does not teach storing data in adjacent memory locations that span a memory boundary with a single header.

Garthwaite et al. discloses compacting a heap memory to remove gaps between live memory objects (Col. 2, lines 35-41) wherein the process of compacting the heap, an object may be relocated to a destination location that causes the object to span two destination blocks after compaction (see Col. 18, lines 20-24; Claim 3; and Figure 6B showing a compacted heap and object 310C spanning block 320A and 320B, object 310F spanning block 320B and 320C, and object 310I spanning block 320D and 320E). In the system of Garthwaite et al. each object contains a single header (see object 450 of Figure 4B) even when stored spanning two blocks of the heap.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of the combination of Eilert in view of Sinclair to include the memory compacting of Garthwaite et al. since doing so avoids fragmentation problems by removing gaps between data objects, thus creating contiguous blocks of available memory and allowing for larger objects to be allocated as well as enabling faster allocation algorithms requiring contiguous free memory (see Col. 2, lines 33-41 of Garthwaite et al.).

Regarding Claim 2, Eilert in view of Sinclair further in view of Garthwaite et al. discloses the memory device wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or

more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 6, Eilert in view of Sinclair further in view of Garthwaite et al. discloses the memory device wherein the block of data comprises system data to be used during system initialization and further wherein the block of data is stored in a pre-selected location within the memory array for all initialization sequences (boot code for initialization is stored within ROM 29, paragraph 0038 of Sinclair).

Regarding Claim 7, Eilert discloses a method comprising:

receiving data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable phase change memory, Col. 1, line 65 – Col. 2, line 6); and control circuitry coupled with the array of memory locations (such as that in processors 52 as shown in Figure 4).

Eilert does not disclose a causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to

one of ordinary skill in the art the time the invention was made to modify the memory of Eilert to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Eilert in view of Sinclair does not teach storing data in adjacent memory locations that span a memory boundary with a single header.

Garthwaite et al. discloses compacting a heap memory to remove gaps between live memory objects (Col. 2, lines 35-41) wherein the process of compacting the heap, an object may be relocated to a destination location that causes the object to span two destination blocks after compaction (see Col. 18, lines 20-24; Claim 3; and Figure 6B showing a compacted heap and object 310C spanning block 320A and 320B, object 310F spanning block 320B and 320C, and object 310I spanning block 320D and 320E). In the system of Garthwaite et al. each object contains a single header (see object 450 of Figure 4B) even when stored spanning two blocks of the heap.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of the combination of Eilert in view of Sinclair to include the memory compacting of Garthwaite et al. since doing so avoids fragmentation problems by removing gaps between data objects, thus creating contiguous blocks of available memory and allowing for larger objects to be allocated as well as enabling faster allocation algorithms requiring contiguous free memory (see Col. 2, lines 33-41 of Garthwaite et al.).

Regarding Claim 8, Eilert in view of Sinclair further in view of Garthwaite et al. discloses the method further comprising causing a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 12, Eilert discloses an article comprising a computer-readable medium having stored thereon instructions that, when executed, cause one or more processors to: receive data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable phase change memory, Col. 1, line 65 – Col. 2, line 6); and control circuitry coupled with the array of memory locations (such as that in processors 52 as shown in Figure 4).

Eilert does not disclose a causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into

two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Eilert to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Eilert in view of Sinclair does not teach storing data in adjacent memory locations that span a memory boundary with a single header.

Garthwaite et al. discloses compacting a heap memory to remove gaps between live memory objects (Col. 2, lines 35-41) wherein the process of compacting the heap, an object may be relocated to a destination location that causes the object to span two destination blocks after compaction (see Col. 18, lines 20-24; Claim 3; and Figure 6B showing a compacted heap and object 310C spanning block 320A and 320B, object 310F spanning block 320B and 320C, and object 310I spanning block 320D and 320E). In the system of Garthwaite et al. each object contains a single header (see object 450 of Figure 4B) even when stored spanning two blocks of the heap.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of the combination of Eilert in view of Sinclair to include the memory compacting of Garthwaite et al. since doing so avoids fragmentation problems by removing gaps between data objects, thus creating contiguous blocks of available memory and allowing for larger objects to be allocated as well as enabling faster allocation algorithms requiring contiguous free memory (see Col. 2, lines 33-41 of Garthwaite et al.).

Regarding Claim 13, Eilert in view of Sinclair further in view of Garthwaite et al. discloses the article further comprising instructions that, when executed, cause the one or more processors to cause a header (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) having an indication of a memory location corresponding to the data fragment to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 25, Eilert discloses a system comprising:

an antenna (for reception and transmission through wireless interface, 56, Fig 4);

a memory system coupled with the antenna, the memory system having an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable phase change memory, Col. 1, line 65 – Col. 2, line 6); and control circuitry coupled with the array of memory locations (such as that in processors 52 as shown in Figure 4).

Eilert does not disclose a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Eilert to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Eilert in view of Sinclair does not teach storing data in adjacent memory locations that span a memory boundary with a single header.

Garthwaite et al. discloses compacting a heap memory to remove gaps between live memory objects (Col. 2, lines 35-41) wherein the process of compacting the heap, an object may be relocated to a destination location that causes the object to span two destination blocks after compaction (see Col. 18, lines 20-24; Claim 3; and Figure 6B showing a compacted heap and object 310C spanning block 320A and 320B, object 310F spanning block 320B and 320C, and object 310I spanning block 320D and 320E). In the system of Garthwaite et al. each object contains a single header (see object 450 of Figure 4B) even when stored spanning two blocks of the heap.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of the combination of Eilert in view of Sinclair to include the memory compacting of Garthwaite et al. since doing so avoids fragmentation problems by removing gaps between data objects, thus creating

contiguous blocks of available memory and allowing for larger objects to be allocated as well as enabling faster allocation algorithms requiring contiguous free memory (see Col. 2, lines 33-41 of Garthwaite et al.).

Regarding Claim 26, Eilert in view of Sinclair further in view of Garthwaite et al. discloses the system wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

4. Claims 3-5, 9-11, 14-16, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eilert (US 6,909,645) in view of Sinclair (US 2007/0088904) further in view of Garthwaite et al. (US 7,389,395) as applied to claims 1-3, 6-9, 12-14, 17-18, 21-22, and 25-27, above, and further in view of Zaidi (US 2006/0245236).

Regarding Claims 3, 9, 14, and 27, Eilert in view of Sinclair further in view of Garthwaite et al. does not teach the memory device wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material. Zaidi

discloses a phase change memory comprising a chalcogenide material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Eilert in view of Sinclair further in view of Garthwaite et al. to include a chalcogenide alloy material in the composition of the phase change memory since this is a well known composition for this type of memory.

Regarding Claims 4, 10, 15, and 28, Zaidi discloses a chalcogenide alloy material comprising GeSbTe (paragraph 0058).

Regarding Claims 5, 11, 16, and 29, Zaidi discloses a chalcogenide alloy material comprising AgInSbTe (paragraph 0058).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185

/Midys Rojas/
Examiner, Art Unit 2185

MR